4601

TTL MICROMATRIX™ ARRAY INTERNAL QUARTER-CELL

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 4601 is a single 4-4 AND-OR-INVERT (AOI) TTμL gate to be used for breadboarding logic designs planned for the 4600 or 4700 Micromatrix™ arrays. The 4601 corresponds to one of the quarter-cell gate elements that are intended for internal (on-chip) usage on the 4600 or 4700 arrays. Standard family TTμL gates such as the 9002 through 9008 may be used to breadboard the quarter-cells having external drive capability. The TTμL 9006 may be used to extend the 4601 at the OR tie points.

FEATURES

- **"INTERNAL" TYPE LOGIC GATES FOR BREADBOARDING 4600 OR 4700 MICROMATRIX ARRAY DESIGNS**
- **CCSL COMPATIBLE**
- **OR EXTENDABLE WITH TTμL 9006**
- **FANOUT = 7 INTERNAL LOADS OR 4.5 EXTERNAL LOADS**
- **"WIRED-AND" OUTPUT CAPABILITY**
- **INPUT CLAMP DIODES FOR RINGING ATTENUATION**

ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential Referenced to Ground	−0.5 V to 7 V
Input Voltage Applied to Input	−0.5 V to 5.5 V
Voltage Applied to Output When Output is High	V_{CC}
Input Current Into Inputs	5 mA
Current Into Output When Output is Low	30 mA
Lead Temperature (soldering, 60 seconds)	300°C

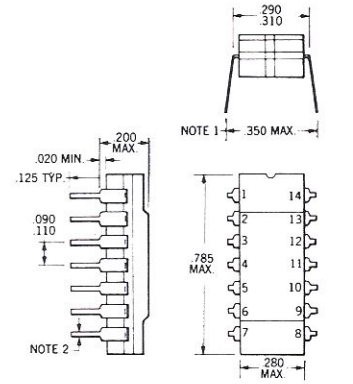
ORDER INFORMATION — Specify A6A46015XX where 5XX is 51X for −55°C to +125°C temperature range and V_{CC} = 5 V ±10%; and 59X for 0°C to 75°C temperature range and V_{CC} = 5 V ±5%.

To order the 4600 Design Kit, specify A6A4600KTX. For the 4700 Design Kit, specify A6A4700KTX.

PHYSICAL DIMENSIONS

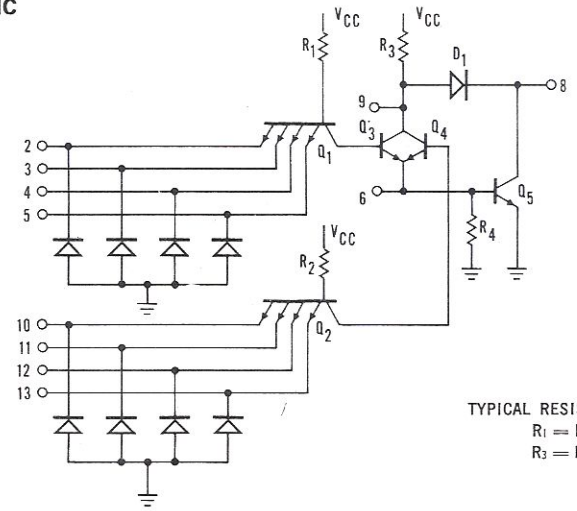
TYPICAL DUAL IN-LINE PACKAGE

In Accordance With
JEDEC (TO-116) Outline



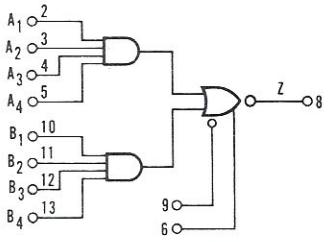
NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

CIRCUIT SCHEMATIC



TYPICAL RESISTOR VALUES
$R_1 = R_2 = 4\ K\Omega$
$R_3 = R_4 = 1.5\ K\Omega$

LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND
PIN 1 = NOT USED

Logic Equation: $Z = \overline{A_1A_2A_3A_4 + B_1B_2B_3B_4 + \ldots}$ *

* More terms are provided with OR extension

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TTL MICROMATRIX™ ARRAY INTERNAL QUARTER-CELL 4601

ELECTRICAL CHARACTERISTICS:

Temperature Range: 0°C to +75°C
Supply Voltage Range: 5 V ±5%

SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 75°C MIN.	LIMITS 75°C MAX.	UNITS	CONDITIONS	
V_{OH}	Output High Voltage	2.3		2.3	2.8		2.3		V	$V_{CC} = 4.75$ V, $I_{OH} = -600\ \mu A$ V_{IL} On Inputs	
V_{OL}	Output Low Voltage Internal Loading		0.6		0.42	0.6		0.6	V	$V_{CC} = 5.25$ V, $I_{OL} = 10.7$ mA $V_{CC} = 4.75$ V, $I_{OL} = 9.3$ mA	
	Output Low Voltage External CCSL Loading		0.4		0.3	0.4		0.4	V	$V_{CC} = 5.25$ V, $I_{OL} = 7.3$ mA $V_{CC} = 4.75$ V, $I_{OL} = 6.4$ mA	
V_{IH}	Input High Voltage	1.9		1.8			1.6		V	Guaranteed Input High Threshold For All Inputs	
V_{IL}	Input Low Voltage		0.8			0.8		0.8	V	Guaranteed Input Low Threshold For All Inputs	
I_F	Input Load Current Internal V_F Level		−1.52		−1.00	−1.52		−1.52	mA	$V_{CC} = 5.25$ V	$V_F = 0.6$ V
			−1.33		−0.87	−1.33		−1.33	mA	$V_{CC} = 4.75$ V	
	Input Load Current External CCSL V_F Level		−1.60		−1.08	−1.60		−1.60	mA	$V_{CC} = 5.25$ V	$V_F = 0.45$ V
			−1.41		−0.91	−1.41		−1.41	mA	$V_{CC} = 4.75$ V	
I_R	Input Leakage Current				5.0	60		60	μA	$V_{CC} = 5.25$ V, $V_R = 4.5$ V	
P_D	Power Dissipation				21	30			mW	Inputs Open	$V_{CC} = 5.0$ V
					11	16			mW	Inputs Grounded	

ELECTRICAL CHARACTERISTICS:

Temperature Range: −55°C to +125°C
Supply Voltage Range: 5 V ±10%

SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS 25°C MIN.	LIMITS 25°C TYP.	LIMITS 25°C MAX.	LIMITS 125°C MIN.	LIMITS 125°C MAX.	UNITS	CONDITIONS	
V_{OH}	Output High Voltage	2.3		2.3	2.55		2.3		V	$V_{CC} = 4.5$ V, $I_{OH} = -600\ \mu A$ V_{IL} On Inputs	
V_{OL}	Output Low Voltage Internal Loading		0.55		0.42	0.55		0.55	V	$V_{CC} = 5.5$ V, $I_{OL} = 10.7$ mA $V_{CC} = 4.5$ V, $I_{OL} = 8.2$ mA	
	Output Low Voltage External CCSL Loading		0.4		0.3	0.4		0.4	V	$V_{CC} = 5.5$ V, $I_{OL} = 7.3$ mA $V_{CC} = 4.5$ V, $I_{OL} = 5.6$ mA	
V_{IH}	Input High Voltage	2.0		1.7			1.4		V	Guaranteed Input High Threshold For All Inputs	
V_{IL}	Input Low Voltage		0.8			0.8		0.7	V	Guaranteed Input Low Threshold For All Inputs	
I_F	Input Load Current Internal V_F Level		−1.52		−1.04	−1.52		−1.52	mA	$V_{CC} = 5.5$ V	$V_F = 0.55$ V
			−1.17		−0.8	−1.17		−1.17	mA	$V_{CC} = 4.5$ V	
	Input Load Current External CCSL V_F Level		−1.60		−1.1	−1.60		−1.60	mA	$V_{CC} = 5.5$ V	$V_F = 0.4$ V
			−1.24		−0.85	−1.24		−1.24	mA	$V_{CC} = 4.5$ V	
I_R	Input Leakage Current				5.0	60		60	μA	$V_{CC} = 5.5$ V, $V_R = 4.5$ V	
P_D	Power Dissipation				21	30			mW	Inputs Open	$V_{CC} = 5.0$ V
					11	16			mW	Inputs Grounded	

LOADING RULES

FAN-OUT (See table):

The internal or "on-chip" fan-out of the 4601 is specified with reduced noise margins since on-chip noise is low. If the 4601 is used specifically for off-chip driving, the maximum fan-out must be reduced to maintain CCSL noise margins.

EXTENSION:

Extension at the 4601 OR extender pins 9 and 6 may be accomplished with TTμL 9006 dual 4 input extender elements. A maximum of 10 extenders (5-9006's) may be tied to the 4601 pins. (See Fig. 1)

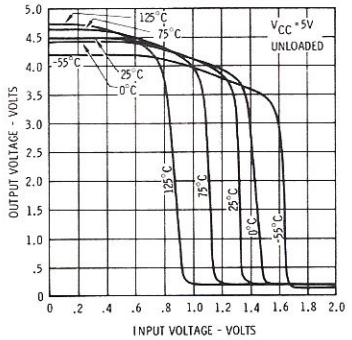
WIRED "AND":
Since the 4601 internal gates have resistive pull-ups, the AND tie of outputs is allowed. (See Fig. 4). Breadboarding of the combined outputs is:
FAN-OUT=7 − (3) (number of outputs tied together − 1)
For "on array" usage optional pull-up resistors allow fan-out as summarized below:

FAN-OUT TABLE

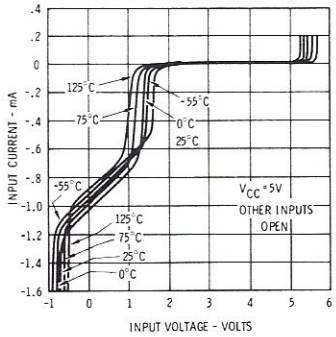
LOADING TYPE	FAN-OUT
INTERNAL	7
TTμL	4.5
DTμL	4.5
LPDTμL	45

TYPICAL INPUT-OUTPUT CHARACTERISTICS

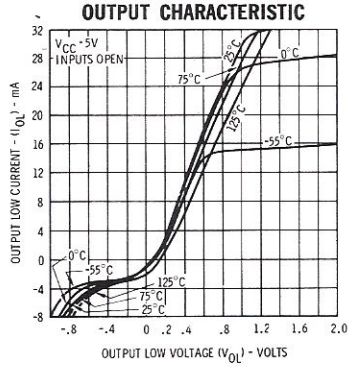
TRANSFER CHARACTERISTIC



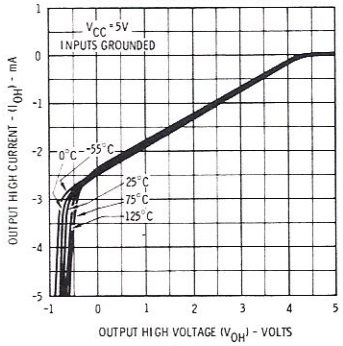
INPUT CHARACTERISTIC



LOW LEVEL OUTPUT CHARACTERISTIC



HIGH LEVEL OUTPUT CHARACTERISTIC



TYPICAL APPLICATIONS

EIGHT INPUT DIGITAL MULTIPLEXER USING "OR" EXTENSION

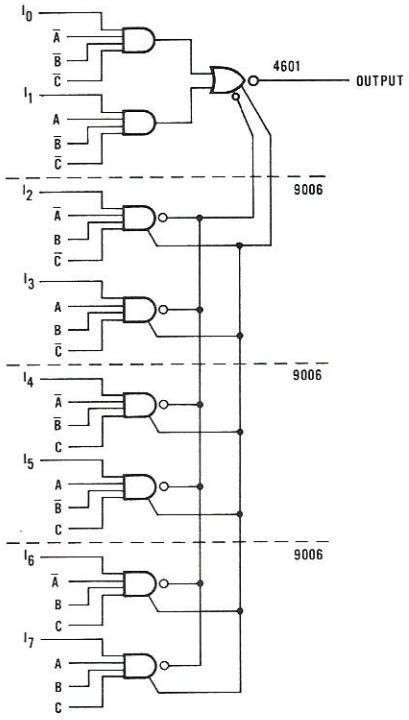


Fig. 1

Three bit address A B C selects an input (I_0, I_1 . . . I_7) which is presented at the output in inverted form. The 4601 is OR-expanded using 3-9006 extender elements.

GATED LATCH USING TWO 4601

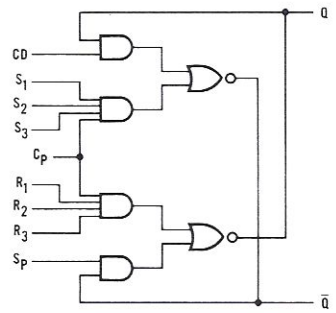
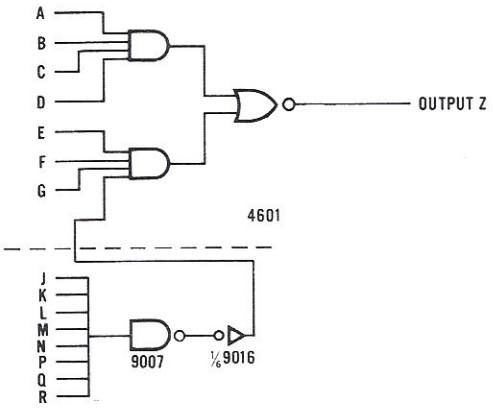


Fig. 2

APPLICATIONS (continued)

INPUT "AND" EXPANSION



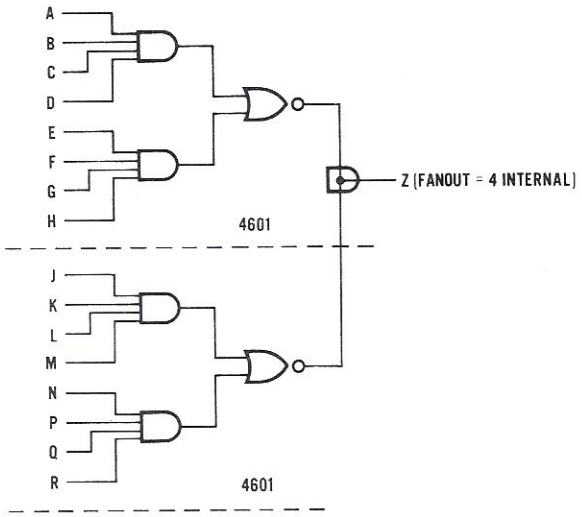
$\overline{Z = ABCD + EFGJKLMNPQR}$

Standard TTμL gates may be used for expansion of "AND" inputs.

*Provision for "AND" expansion is made on the micromatrix array thru "selective bar" options.

Fig. 3

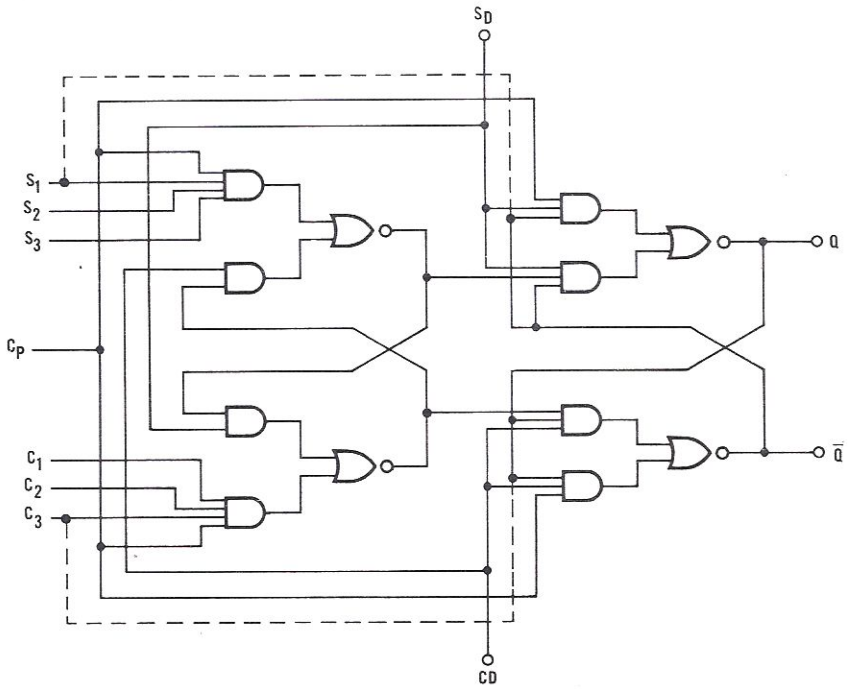
WIRED "AND"



$Z = \overline{[ABCD + EFGH]} \cdot \overline{[JKLM + NPQR]}$

Fig. 4

GENERAL PURPOSE MASTER-SLAVE FLIP-FLOP USING FOUR 4601



For J-K operation, connect as shown in dotted lines. The outputs change on the high to low clock transition.

Fig. 5

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